



INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁶ :

H01L 27/146

A1

(11) International Publication Number:

WO 98/57376

(43) International Publication Date:

17 December 1998 (17.12.98)

(21) International Application Number: PCT/US98/11900

(22) International Filing Date: 9 June 1998 (09.06.98)

(30) Priority Data:

08/873,123

11 June 1997 (11.06.97)

US

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(81) Designated States: CA, JP, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published

With international search report.

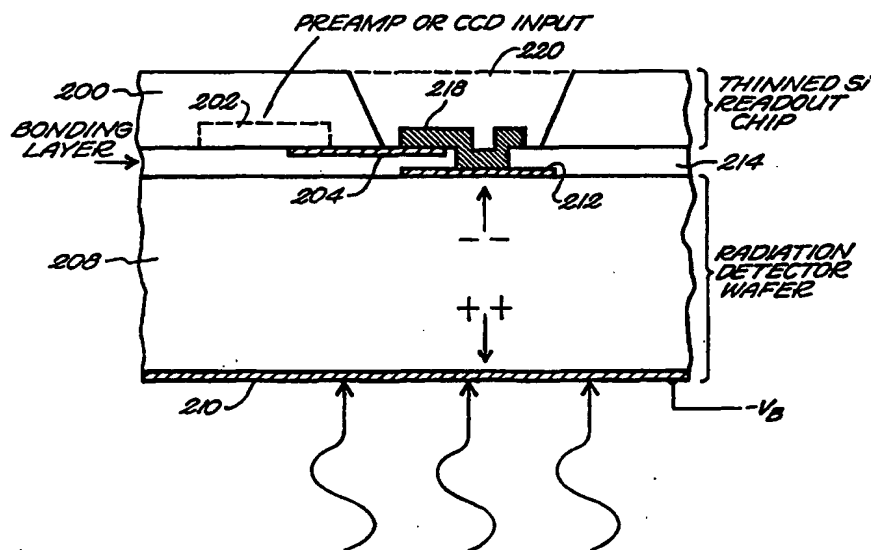
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

FP00-0050-00EP-HP

04.3.5

SEARCH REPORT

(54) Title: INTERCONNECTION TECHNIQUE FOR HYBRID INTEGRATED DEVICES



(57) Abstract

A hybrid integrated circuit and method of fabricating a hybrid integrated circuit. A first wafer (200) is provided having a first surface with a first electrical contact (204) for a first active circuit associated therewith and a second surface. A second wafer (208) is provided having a third surface with a second electrical contact (212) for a second active circuit associated therewith and a fourth surface, the second wafer being chemically thinned at the fourth surface. The first and second wafers are bonded together at an interface (214) between the first and third surfaces such that the first and second electrical contacts are relatively aligned with one another. The fourth surface of the second wafer is processed to define an access (220) via to both the first and second contacts. An electrical interconnection (218) is formed between the first and second contacts within the access via so that the first and second active circuits are electrically interconnected.

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INTERCONNECTION TECHNIQUE FOR HYBRID INTEGRATED DEVICES

This invention was made with government support under Contract No. F19628-95-C-0002 awarded by the U.S. Air Force.
5 The government has certain rights in the invention.

BACKGROUND OF THE INVENTION

The invention relates to interconnecting semiconductor devices to fabricate hybrid integrated circuits.

10 Hybrid integrated circuits are an important class of circuits in which two or more devices, or possibly dissimilar materials, are interconnected to perform a function that is not feasible with a monolithic device. Typically, connections are made to the devices using wire
15 bonding to pads arranged around the perimeter of the device. Other methods such as automated tape bonding and beam leads, are also limited to contacts being made to the periphery of the device.

For some time it has been realized that applications
20 exist for which the method of attaching leads around the edge of the device is inadequate. Primary examples are imaging arrays, in which a photosensitive array is bonded to a second device that performs amplification and readout functions, and random logic functions in which the number of
25 signal leads are too large to be placed all along the perimeter of the device. The most common approach to imaging arrays is the use of indium bump bonding, which does not require the use of elevated temperatures. For random logic functions applications the technology of solder bumps
30 has been widely employed.

Hybrid imaging arrays are an important use of indium bump bonding for medium-and far-infrared detection, as well as potentially the hard x-ray and gamma-ray region. In these portions of the spectrum ($\lambda > 1000$ nm and $\lambda < 0.1$ nm,
35 respectively) silicon itself has no useful response, while the materials that are sensitive in these regimes (HgCdTe, InSb, CdTe, HgI etc.) lack a well-developed and high-yield technology for integrated readout circuitry. Although it

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has been in development for many years, the indium bump-bonding approach is thought to be expensive and difficult to perform, and for large arrays involving thousands of bumps the probability is very high that at least a few bumps will fail to make electrical connection.

Another approach to the problem is to grow the radiation-sensitive material directly on the silicon readout chip. This has several problems, such as compatibility between the epilayer growth conditions and the silicon device, the generally inferior quality of heteroepitaxially grown material compared to homoepitaxially or bulk-grown material, and limitations on the practical thickness of the epitaxial layers. The latter is particularly important for hard x-ray and gamma-ray imaging, where the detector material may need to be hundreds of μm thick for useful sensitivity.

SUMMARY OF THE INVENTION

Accordingly the invention provides a hybrid integrated circuit and method of fabricating a hybrid integrated circuit. A first wafer is provided having a first surface with a first electrical contact for a first active circuit associated therewith and a second surface. A second wafer is provided having a third surface with a second electrical contact for a second active circuit associated therewith and a fourth surface, the second wafer being chemically thinned at the fourth surface. The first and second wafers are bonded together at an interface between the first and third surfaces such that the first and second electrical contacts are relatively aligned with one another. The fourth surface of the second wafer is processed to define an access via to both the first and second contacts. An electrical interconnection is formed between the first and second contacts within the access via so that the first and second active circuits are electrically interconnected.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGs. 1A-1F illustrate in cross section a back-

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illuminated silicon process to fabricate a CCD imager; and
FIGs. 2A-2D illustrate in cross section a process of
fabricating a hybrid integrated circuit and the resulting
hybrid integrated circuit with massively parallel
5 interconnections.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

The present invention involves a new approach for
hybrid device fabrication that features massively parallel
10 interconnections and potentially higher yield and greater
ease of manufacturing. The approach is an extension of the
precision thinning and bonding technology, which has been
used extensively to make back-illuminated (BI) silicon CCD
imaging detectors. The BI process is described in Huang et
15 al., "A New Process for Thinned, Back-Illuminated CCD Imager
Devices", International Symposium on VLSI Technology Systems
and Applications (1989), incorporated herein by reference.

FIGs. 1A-1F illustrate in cross section the BI process
as is currently practiced for CCD imagers. An active device
20 wafer 10 such as a front illuminated wafer assembly, having
an active circuit 12 and electrical contact 14, is
chemically thinned to as little as a few μm thickness and
treated in accordance with a conventional thinning process
as shown in FIGs. 1A-1C. The thinned active wafer 10 is
25 then bonded to an electrically inactive support/carrier
substrate wafer 16 with an epoxy layer 18 as shown in FIG.
1D. A further etching step removes the silicon above the
metallic electrical contact 14 to create an access via 20 as
shown in FIG. 1E. In addition, deposits forming a light
30 shield and antireflection coating are provided to complete
the device.

At this point in the fabrication process, the
electrical contact 14, which was previously on the top of
the non-thinned active wafer 10, is now separated from the
35 carrier wafer by about $5\mu\text{m}$ of epoxy layer 18 and
approximately $2\mu\text{m}$ of scratch-prevention glass. In the
present practice, the carrier wafer is passive electrically
and acts as a mechanical support only, and the contact 14 is

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wire-bonded via lead 22 to a package.

In accordance with the present invention, the active device wafer to be thinned is bonded to another active device wafer having a photosensitive array or a logic device
5 rather than a carrier wafer having no purpose other than support. The device to be thinned and bonded can be any silicon circuit such as CCD imagers or Si microprocessor circuits.

FIGs. 2A-2D illustrate an exemplary semiconductor
10 device with an imaging application fabricated in accordance with the invention. FIG. 2A shows a first active device wafer 200. The wafer is a conventional silicon wafer having an active circuit 202 configured on an active surface 203 thereof. The active circuit can be fabricated by
15 conventional methods of epitaxial layer growth, ion implantation and diffusion as is well known to those of skill in the art. For purposes of illustrating the invention, the active circuit 202 is the input region of a CCD or preamplifier device of a readout circuit or readout
20 chip. The active circuit has associated therewith electrical contacts 204, which are made for example by conventional metal evaporation techniques. The wafer 200 is thinned on the opposite surface 206 in accordance with conventional thinning techniques as described above.

25 A second active device wafer 208 of a desired radiation-sensitive material, such as CdTe for hard x-rays or HgCdTe for the far infrared, has a continuous bias electrode 210 configured on the bottom portion of the wafer. An electrode array of electrical contacts 212 is provided on the upper
30 surface thereof, each contact corresponding to the desired individual pixels of the imaging array. The wafer 208 in the illustrated example corresponds to a radiation detection wafer.

FIG. 2B shows the first active device wafer 200 being
35 bonded to the second active device wafer 208 in a conventional manner with a bonding layer 214. The bonding layer comprises a non-conductive epoxy or oxide based adhesive which serves to adhere the wafers together and to

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electrically isolate the circuits associated with each wafer. During the bonding process, the first and second wafers are aligned such that the electrical contacts 204 of the first wafer are in proximity to the corresponding 5 electrical contacts 212 of the second wafer.

In accordance with FIG. 2C, the thinned silicon wafer, any oxide layers and epoxy over each detector electrode are etched away in a conventional manner to form an access via 216 exposing both an contact 212 of the second active device 10 wafer and its corresponding contact on the first active device wafer.

As shown in FIG. 2D, a metal electrode 218 connecting the contacts 204 and 212 can then be deposited within the via 216. Thereafter, an insulating layer 220 such as an 15 oxide layer is provided to electrically insulate and isolate the connecting electrode 218. The resulting assembly is a hybrid integrated circuit, in the illustrated example a hybrid radiation detector, in which the active devices on each of the bonded wafers are interconnected in parallel on 20 a massive scale, depending on the number of connections required. In the illustrated example, the radiation detector would require interconnections at each pixel location.

The benefits of this technology over the conventional 25 bump bonding technology are as follows. The massively parallel interconnection process of the invention results in higher yields of devices. The invention provides an opportunity to rework individual bonds or the entire array if the first attempt is not successful, in contrast to bump- 30 bonding schemes. The invention results in higher density of bonds. The physical size of the bond area will be approximately the same as the thickness of the thinned wafer plus the bonding layer (typically less than 20 μm total). In addition, the invention provides for the possibility of 35 multi-layer circuits. The same procedure can be repeated with a third layer using the two-device layer as a substrate, etc.

It will be appreciated that the interconnection process

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and resulting hybrid circuits are not limited to the specific hardware examples provided herein for purposes of illustrating the invention. The interconnection technique of the invention is intended for use with any number of 5 wafers having active circuits thereon requiring electrical interconnections.

The foregoing description has been set forth to illustrate the invention and is not intended to be limiting. Since modifications of the described embodiments 10 incorporating the spirit and substance of the invention may occur to persons skilled in the art, the scope of the invention should be limited solely with reference to the appended claims and equivalents thereof.

15 What is claimed is:

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CLAIMS

1 1. A method of fabricating a semiconductor device,
2 comprising:

3 providing a first wafer having a first surface with a
4 first electrical contact associated therewith and a second
5 surface;

6 providing a second wafer having a third surface with a
7 second electrical contact associated therewith and a fourth
8 surface, said second wafer being thinned at said fourth
9 surface;

10 coupling said first and second wafers together at an
11 interface between said first and third surfaces such that
12 said first and second electrical contacts are relatively
13 aligned with one another;

14 processing said fourth surface of said second wafer to
15 define an access via to both said first and second contacts;
16 and

17 forming an electrical interconnection between said
18 first and second contacts within said access via.

1 2. The method of claim 1, further comprising the step
2 of providing an insulative layer over said electrical
3 interconnection within said access via.

1 3. The method of claim 1, wherein said electrical
2 interconnection comprises a metallic electrode.

1 4. The method of claim 1, wherein said first wafer
2 comprises a radiation detector device.

1 5. The method of claim 4, wherein said second wafer
2 comprises a readout chip.

1 6. A method of fabricating a hybrid integrated
2 circuit, comprising:

3 providing a first wafer having a first surface with a
4 first electrical contact for a first active circuit

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5 associated therewith and a second surface;
6 providing a second wafer having a third surface with a
7 second electrical contact for a second active circuit
8 associated therewith and a fourth surface, said second wafer
9 being chemically thinned at said fourth surface;
10 bonding said first and second wafers together at an
11 interface between said first and third surfaces such that
12 said first and second electrical contacts are relatively
13 aligned with one another;
14 processing said fourth surface of said second wafer to
15 define an access via to both said first and second contacts;
16 and
17 forming an electrical interconnection between said
18 first and second contacts within said access via so that
19 said first and second active circuits are electrically
20 interconnected.

1 7. The method of claim 6, wherein said first wafer
2 comprises a radiation detector device.

1 8. The method of claim 7, wherein said second wafer
2 comprises a readout chip.

1 9. The method of claim 8, wherein said hybrid
2 integrated circuit comprises a hybrid radiation detector.

1 10. A hybrid integrated circuit, comprising:
2 a first wafer having a first surface with a first
3 electrical contact for a first active circuit associated
4 therewith and a second surface;
5 a second wafer having a third surface with a second
6 electrical contact for a second active circuit associated
7 therewith and a fourth surface, said second wafer being
8 chemically thinned at said fourth surface, said first and
9 second wafers being bonded together at an interface between
10 said first and third surfaces such that said first and
11 second electrical contacts are relatively aligned with one
12 another;

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13 an access via to both said first and second contacts
14 from said fourth surface; and

15 an electrical interconnection between said first and
16 second contacts within said access via so that said first
17 and second active circuits are electrically interconnected.

1 11. The method of claim 10, wherein said first wafer
2 comprises a radiation detector device.

1 12. The method of claim 11, wherein said second wafer
2 comprises a readout chip.

1 13. The method of claim 12, wherein said hybrid
2 integrated circuit comprises a hybrid radiation detector.

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FRONT ILLUMINATED WAFER

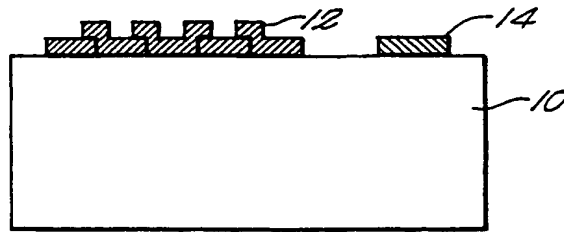


FIG. 1A

THIN (EXCEPT FOR RIM SUPPORT)

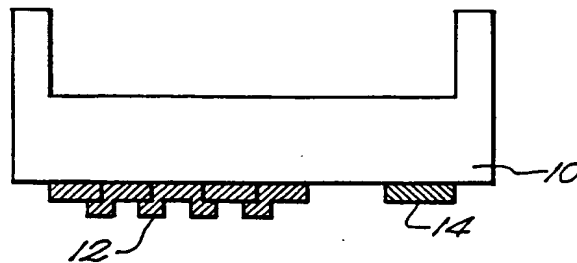


FIG. 1B

TREAT BACK SURFACE
DEPOSIT, ANNEAL

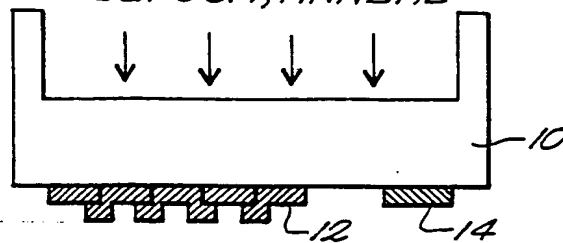
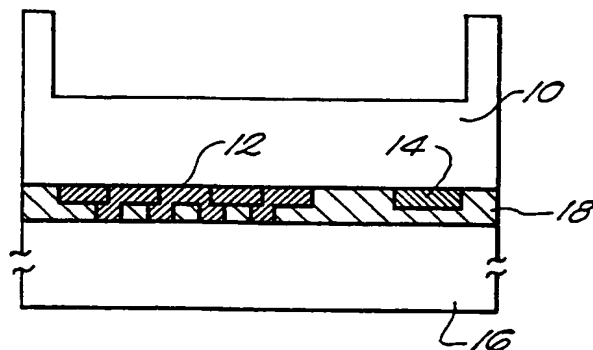
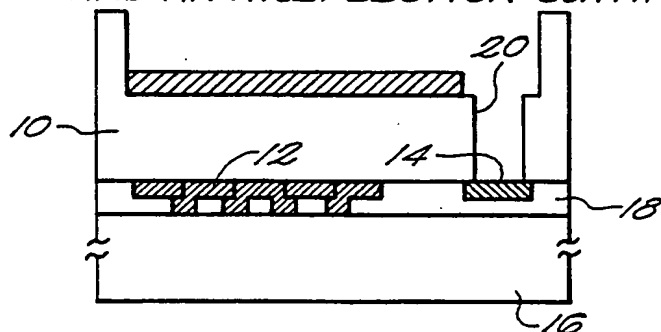


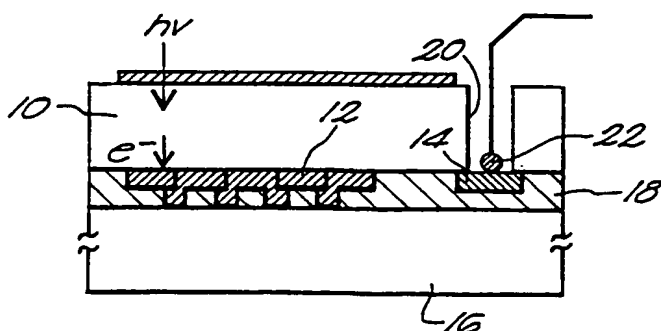
FIG. 1C

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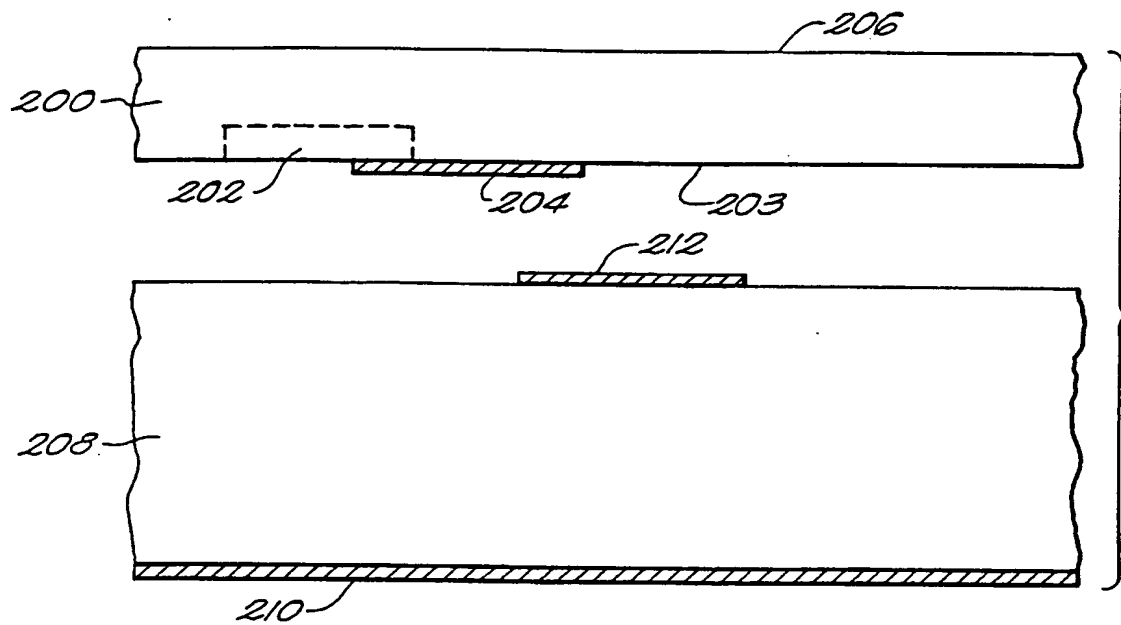
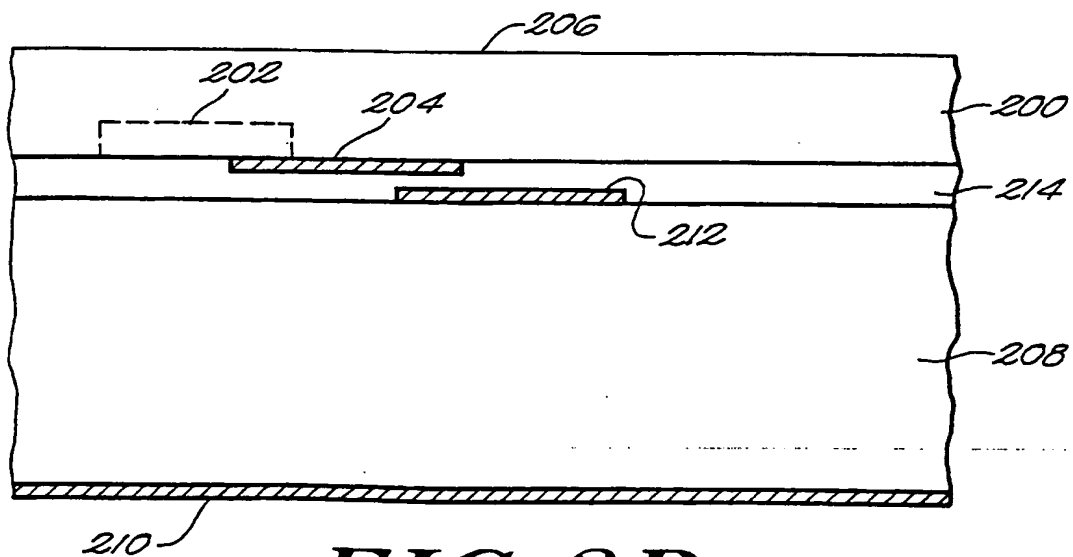
BOND TO SUBSTRATE

**FIG. 1D**ETCH VIAS, DEPOSIT LIGHT SHIELD
AND ANTIREFLECTION COATING**FIG. 1E**

PACKAGE DEVICE

**FIG. 1F**

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**FIG. 2A****FIG. 2B**

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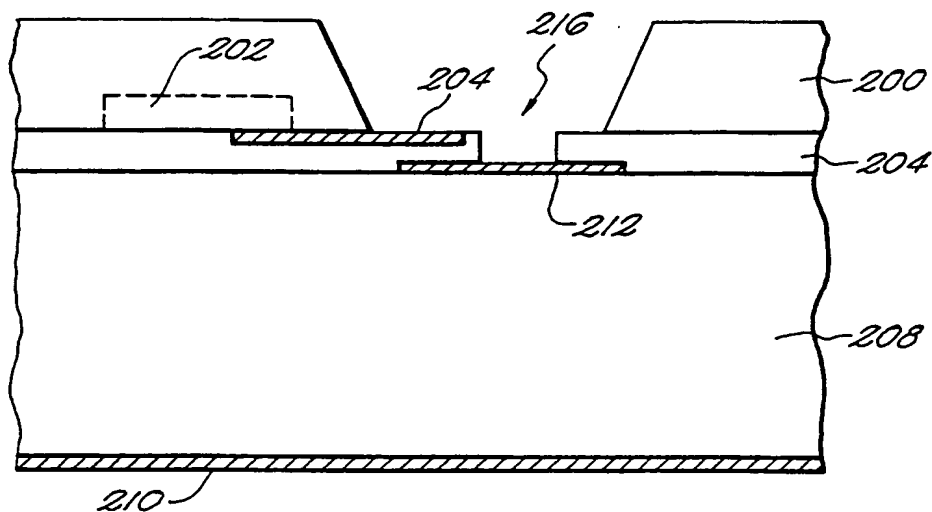


FIG. 2C

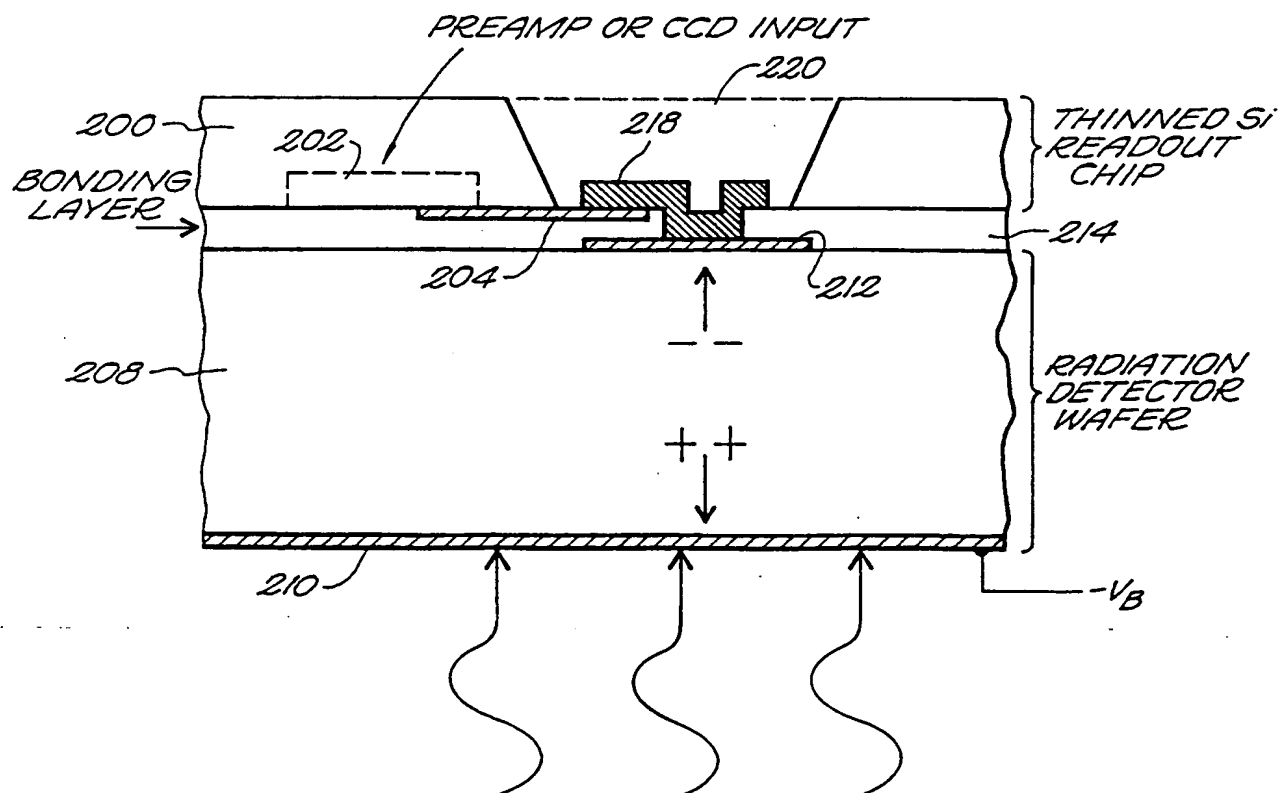


FIG. 2D

INTERNATIONAL SEARCH REPORT

In .tional Application No

PCT/US 98/11900

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L27/146

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 773 436 A (ROCKWELL INTERNATIONAL CORP) 14 May 1997 see figures 5A-5E see column 3, line 12 - line 48 see column 7, line 26 - column 9, line 14	1-3, 6, 10
Y	---	4, 5, 7-9, 11-13
Y	US 4 547 792 A (SCLAR NATHAN) 15 October 1985 see abstract; figures 6, 7 see column 3, line 51 - column 4, line 13 see column 4, line 67 - column 5, line 46 --- -/--	4, 5, 7-9, 11-13

☒ Further documents are listed in the continuation of box C.☒ Patent family members are listed in annex.

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Date of the actual completion of the international search

18 September 1998

Date of mailing of the international search report

06/10/1998

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INTERNATIONAL SEARCH REPORT

In International Application No

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication where appropriate, of the relevant passages	Relevant to claim No.
A	<p>HUANG C M ET AL: "A new process for thinned, back-illuminated CCD imager devices"</p> <p>1989 INTERNATIONAL SYMPOSIUM ON VLSI TECHNOLOGY, SYSTEMS AND APPLICATIONS. PROCEEDINGS OF TECHNICAL PAPERS (CAT. NO.89CH2631-0), TAIPEI, TAIWAN, 17-19 MAY 1989, pages 98-101, XP002078066</p> <p>1989, New York, NY, USA, IEEE, USA</p> <p>cited in the application</p> <p>see abstract; figure 1</p> <p>see paragraph 2</p> <p>---</p>	1-13
A	<p>US 4 104 674 A (LORENZE JR ROBERT V ET AL)</p> <p>1 August 1978</p> <p>see abstract; figure 1B</p> <p>see column 1, line 19 - line 56</p> <p>see column 1, line 62 - column 2, line 9</p> <p>see column 2, line 58 - column 3, line 23</p> <p>-----</p>	1,3-13

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

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